III. REMARKS

Claims 1 and 3-31 are pending in this application. By this Supplemental Amendment, claim 1 and 3 have been amended and claim 2 has been cancelled. Reconsideration in view of the following remarks is respectfully requested.

This application claims priority to International Appln. Serial No. PCT/US2003/05314, hereinafter "'05314." Accordingly, Applicants respectfully direct the Office's attention to the International Preliminary Examination Report, submitted herewith for reference, for '05314. In the examination report, the examining office has indicated a favorable determination with respect to novelty, inventive step and industrial applicability. Examination report, p. 4. As a result, Applicants have amended the claims in the present application to duplicate the claims as examined in the examination report. Applicants submit that claims 1 and 3-31 are allowable and respectfully request that the Office defer to the determination reached in the examination report.

Furthermore, Applicants respectfully request that the Office's previous restriction requirement and species requirement be withdrawn in light of the search performed in connection with '05314. See MPEP §803, in which it is stated that "[i]f the search and examination of an entire application can be made without serious burden, the Examiner must examine it on the merits, even though it includes claims to independent or distinct inventions" (emphasis added). Applicants respectfully submit that there can be no serious burden on the Office because the search has already been completed. Accordingly, Applicants respectfully request withdrawal of both the Restriction and Species Election Requirements.

IV. CONCLUSION

In light of the above, Applicants respectfully submit that all claims are in condition for allowance. Should the Examiner require anything further to place the application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the number listed below.

Respectfully submitted,

/Darrell L. Pogue/

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Date: October 26, 2006

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PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
STEVEN J. SOUCAR SPA
INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G, BLDG. 300/482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	18 APR 2006
Applicant's or agent's file reference BUR920020068	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US03/05314	20 February 2003 (20.02.2003)	12 December 2002 (12.12.2002)

Applicant

INTERNATIONAL BUSINESS MACHINES CORPORATION

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

2006 APR 24 A 8:12 IBM

Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Evan Pert Telephone No. 308-0956

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference BUR920020068	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US03/05314	International filing date *(day/month/year)* 20 February 2003 (20.02.2003)	Priority date *(day/month/year)* 12 December 2002 (12.12.2002)
International Patent Classification (IPC) or national classification and IPC IPC(7): G01R 31/26 and US Cl.: 324/765		
Applicant INTERNATIONAL BUSINESS MACHINES CORPORATION		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

☒ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of 8 sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
09 July 2004 (09.07.2004)	09 February 2006 (09.02.2006)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/ US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Evan Pert Telephone No. 308-0956

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US03/05314

I. Basis of the report

1. With regard to the **elements** of the international application:*

☐ the international application as originally filed.

☒ the description:
pages 1-32 as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of .

☒ the claims:
pages NONE , as originally filed
pages 33-40 , as amended (together with any statement) under Article 19
pages NONE , filed with the demand
pages NONE , filed with the letter of .

☒ the drawings:
pages 1/4 to 4/4 , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of .

☐ the sequence listing part of the description:
pages NONE , as originally filed
pages NONE , filed with the demand
pages NONE , filed with the letter of .

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language English which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☒ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☐ the description, pages NONE

☒ the claims, Nos. 33

☐ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US03/05314

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1-32	YES
	Claims NONE	NO
Inventive Step (IS)	Claims 1-32	YES
	Claims NONE	NO
Industrial Applicability (IA)	Claims 1-32	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS

Claims 1-30 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest the method limitations drawn to separately adjusting well bias for an n-transistor and p-transistor wired separately from circuit VDD and ground, with partitions among transistors allowing individual adjustments, or using voltage-based testing (unlike IDDQ, for example), while claims 31-32 set forth a novel system, particularly for self-regulation of burn-in temperature combined with well bias being wired independently for an n-transistor and p-transistor, and wired separately from ground.

Claims 1-32 meet the criteria set out in PCT Article 33(4), and thus have industrial applicability because the subject matter claimed can be made or used in industry.

While the SACHDEV reference was cited as an "X" reference in the International Search Report, this reference does not disclose that the "wells are wired separately from circuit VDD and ground," for example, which was overlooked at the time the Search Report was prepared.

While the TOSUKA ET AL. reference was cited as an "X" reference in the Intrenational Search Report, this reference is not an invention "for testing" while some limitations of the claims are arguably disclosed.

Claims

1. A method for testing an integrated circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the method comprising the steps of:

testing a circuit including independently modifying a p-well (14) bias of an n-transistor (16) and an n-well bias (18) of a p-transistor (20); and

determining whether a defect exists from the testing;

wherein the wells (14, 18) include partitions, the modifying step includes applying a different well bias condition to at least one partition compared to at least one other partition, and the determining step is applied to one of the circuit as a whole and on a partition-by-partition basis.

2. The method of claim 1, wherein the modifying step includes applying a plurality of different well bias conditions to a plurality of different partitions, and the determining step includes comparing the results of the testing to one another to localize a defect.

3. The method of claim 1, wherein the testing step further includes stimulating the circuit with a test vector followed by the step of modifying the well biases for a predetermined time prior to the determining step.

4. The method of claim 1, wherein the determining step includes comparing outputs of the circuit to expected results for a defect-free circuit.

5. The method of claim 1, wherein the determining step includes comparing outputs of the circuit to results for the same circuit under different well bias conditions.

6. The method of claim 1, wherein the testing includes modifying the well biases to one of a plurality of extreme conditions.

7. The method of claim 6, wherein the determining step includes observing a circuit parameter in addition to well bias during the testing.

8. The method of claim 6, wherein the testing step further includes modifying at least one circuit parameter other than well bias.

9. The method of claim 1, wherein the testing step further includes voltage-based testing.

10. The method of claim 10, wherein the modifying step includes one of:

(a) decreasing a p-well (14) bias for the n-transistor (16) and decreasing an n-well (18) bias for the p-transistor (20);

(b) increasing the p-well bias for the n-transistor and increasing the n-well bias for

the p-transistor; and

(c) increasing the p-well bias for the n-transistor and decreasing the n-well bias for

AMENDED SHEET

the p-transistor.

11. The method of claim 10, wherein the voltage-based testing includes applying a low-VDD.

12. The method of claim 10, wherein the modifying step includes:

first setting each well bias at a nominal value;

second increasing the p-well (14) bias of the n-transistor (16) from a nominal value and setting the n-well (18) bias of the p-transistor (20) at a nominal value; and

third setting the p-well bias of the n-transistor at a nominal value and decreasing the n-well bias of the p-transistor from a nominal value,

wherein the determining step occurs between each of the above steps.

13. The method of claim 13, wherein the modifying step further includes:

fourth setting the p-well (14) bias of the n-transistor (16) to a lower than nominal value and the n-well (18) bias of the p-transistor (20) to a higher than nominal value;

fifth setting the p-well bias of the n-transistor to a lower than nominal value and the n-well bias of the p-transistor to a lower than nominal value;

sixth setting the p-well bias of the n-transistor to a higher than nominal value and the n-well bias of the p-transistor to a higher than nominal value,

wherein the determining step occurs between each of the above steps.

AMENDED SHEET

14. The method of claim 10, wherein the determining step includes determining at least one of a minimum well bias and a maximum well bias at which the IC (10) functions at a particular speed; and determining whether at least one minimum and maximum well bias meets a predetermined goal.

15. The method of claim 1, wherein the testing includes measuring an elevated static leakage current (IDDQ).

16. The method of claim 16, wherein the modifying step includes applying both increases and decreases of well bias to establish a relationship between IDDQ and well bias.

17. The method of claim 16, wherein the step of applying includes:

applying a first set of biases to the n-well (18) and the p-well (14), and then measuring IDDQ; and

applying a different second set of biases to the n-well and the p-well, and then measuring IDDQ.

18. The method of claim 16, wherein the determining step includes comparing the results of the applying step to expected results for a defect-free circuit.

19. The method of claim 16, wherein the determining step includes:

establishing an IDDQ curve shape for a defect-free circuit from the applying

AMENDED SHEET

steps;

establishing an IDDQ curve shape for a circuit under test; and

comparing the curve shapes.

20. The method of claim 16, wherein the modifying step includes setting a well bias to at least substantially decrease one type of IDDQ, and the step of determining includes performing a characterization of the other type of IDDQ versus at least one circuit parameter.

21. The method of claim 1, wherein the testing includes stress testing.

22. The method of claim 22, wherein the modifying step includes modifying well bias to modify switching current.

23. The method of claim 22, wherein the modifying step includes modifying well bias to modify current during at least one of burn-in stressing and high-voltage stressing.

24. The method of claim 22, wherein the modifying step includes modifying well bias to draw a predetermined amount of at least one of switching and static current.

25. The method of claim 22, wherein the modifying step includes:

increasing the p-well bias and decreasing the n-well bias when circuit switching is to occur; and

AMENDED SHEET

decreasing the p-well bias and increasing the n-well bias when circuit switching is not to occur.

26. The method of claim 22, wherein the modifying step includes setting well-bias at a first setting during high voltage burn-in and a second setting during nominal voltage burn-in.

27. The method of claim 22, wherein the modifying step includes setting well-bias during burn-in to maintain circuit functioning.

28. The method of claim 22, wherein the modifying step includes setting well-bias to maintain a stress test temperature.

29. The method of claim 22, wherein the modifying step includes modifying well bias during stressing to accelerate defects by placing an elevated electric field across a gate oxide of the circuit.

AMENDED SHEET

PAGE 11/13 * RCVD AT 11/21/2005 3:50:40 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2733201 * CSID:518 449 0047 * DURATION (mm-ss):02-44

30. A method for testing a semiconductor circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the method comprising the steps of:

testing the circuit for a defect by measuring static leakage current; and

increasing and decreasing well biases of an n-transistor (16) and a p-transistor (20) to change respective transistor threshold voltages during testing.

31. A system for testing a semiconductor circuit (10) having wells (14, 18) that are wired separately from circuit VDD and ground, the system comprising:

means for testing (60) the circuit including independently modifying a well bias of an n-transistor (16) and a well bias of a p-transistor (20); and

means for determining (62) whether a defect exists from the testing;

wherein the wells (14, 18) include partitions, the well bias modifying includes applying a different well bias condition to at least one partition compared to at least one other partition, and the determining is applied to one of the circuit as a whole and on a partition-by-partition basis.

32. The system of claim 32, further comprising a temperature sensor (50, 52) for monitoring a temperature of the IC, wherein the means for testing (60) modifies the well biases to maintain a stress test temperature.

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PAGE 13/13 * RCVD AT 11/21/2005 3:59:40 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/27 * DNIS:2733201 * CSID:518 449 0047 * DURATION (mm-ss):02-44